EE/CprE/SE 492 Status Report 1
Jan 20– Feb 5

Group number: **22**

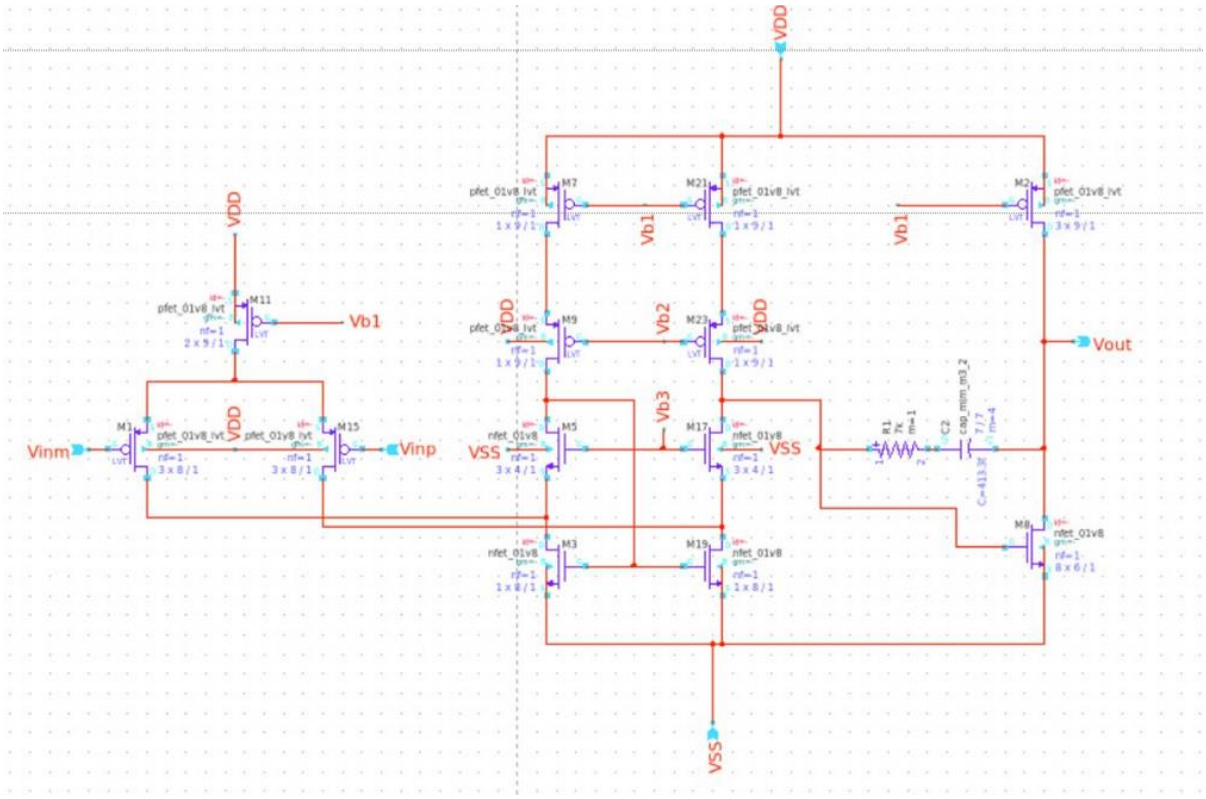
Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - Significant progress into completing the project. ReRAM instantiated in layout, 1T1R layout progress, need routing and LVS passing still, TIA design settled on (currently working on transistor sizing and bias voltages), ADC design started. Chipfoundry recently updated CLI tool, exploring usability and benefits.
- **Past week accomplishments**
  - Vinicius Malaman Soares: Set up for in person group work. Imported past team git repositories to test out Data Converters.
  - Tyler Kloser: Looked through our current designs and compared them to previous ReRAM teams to understand how are main designs are different in terms of specific files from Skywater PDK. Practiced putting previous repos through layout and simulation. Looked at opamp, 4bitADC, and analogMUX.
  - Ali Mannan: Design for transimpedance amplifier underway, two-stage operational amplifier with bias voltages to be decided. Attached is an illustration of the design.



- Austin Miller: Looked into updated documentation from Chipfoundry regarding harness types, GPIO differences and past issues from Efabless repos. Explored new Chipfoundry CLI tool to allow more uniformity and easier toolflow (librelane hardening, precheck, gpio configs). 1T1R somewhat in magic, unsure of LVS though.

- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: N/A
  - Austin Miller: Unsure that reram cell will behave and link to schematic cell as intended currently. CLI tool installs weird – trying on fresh vm's
  - Vinicius Malaman Soares: N/A

- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Tyler Kloser	Practiced layout in Magic and looked at other teams repos into possible design ideas	6	6
Ali Mannan	Transimpedance amplfier design	10	10
Austin Miller	Harness Comparisons (and clarifications), CLI Tool exploration	14	14
Vinicius Malaman Soares	Clone pass teams repos and test out	6	6

- **Comments and extended discussion**
    - N/A

Plans for the upcoming week

- Ali Mannan: Layout of operational amplifier, intend to help other group members with Magic VLSI layout tools when other layouts are ready to be done
- Tyler Kloser: Work with the team to figure out what I can do and keep learning more about how to use Magic. Look at current opamp design. Test designs that might be useful from previous teams repos.
- Austin Miller: Get 1T1R layout done, check whether that or even simple inverter can get through precheck in our current tool setup. Hopefully get CLI tool to work for our methods.
- Vinicius Malaman Soares: Test the components that can be used in depth.

- **Summary of weekly advisor meeting**
    - The exact model of the final tapeout was discussed in detail with the client. It was made sure that the Caravel harness is the one we will be using, and not the more analog/high-speed Caravan harness. Went into more depth on differences on GPIO pins and their analog setups such as bare pads (Caravan), 150-ohm analog, or no-esd analog. Will try and make tests to possibly see if one is drastically different. We also discussed additional details on the process of submitting the final design for manufacturing.